UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/878,497 | 06/11/2001 | Attila Kovacs-Birkas | M-11510 US | 3073 |

33031 7590 02/24/2005

CAMPBELL STEPHENSON ASCOLESE, LLP
4807 SPICEWOOD SPRINGS RD.
BLDG. 4, SUITE 201
AUSTIN, TX 78759

| EXAMINER | |
|---|---|
| THOMSON, WILLIAM D | |
| **ART UNIT** | **PAPER NUMBER** |
| 2123 | |

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/878,497 | KOVACS-BIRKAS, ATTILA | |
| | Examiner | Art Unit | |
| | William D. Thomson | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

**1.** Claims 1-23 have been presented for reconsideration in view of Applicants amended claims language and arguments.

### ***Response to Arguments***

**2.** Applicants arguments submitted in the 11-26-2004 responses have been fully considered. The Examiners response is as follows.

**2.1** Regarding the Applicant's amendment to the specification.

The Examiner thanks the Applicant for the amendment to the specification and withdraws the earlier objection to the same.

**2.2** Regarding the Applicant's response to the 35 U.S.C. § 102(2) rejections of claims 1-23.

Applicant argued,

> However, the Office Action does not indicate that Gan teaches or fairly suggests that a standard block 210 and phantom block 220, 230 are components of an input/output cell as required of claim 1.

The Examiner respectfully traverses the Applicants argument. The Examiner notes that the *Gan et al.* reference is directed towards the placement of I/O ports, specifically *Gan et al.* teaches, ***(Col. 5 lines 19-20,*** *The phantom blocks define the I/O ports and connectivity of the custom blocks to be implemented.)*

Applicant further argued,

> Accordingly, stopper cells cannot act as a cover and prevent an area occupied by phantom block 220, 230 from being used for any purpose other than occupation by phantom block 220, 230. Accordingly, Applicants submit that independent claim 1 is patentably distinguishable over Gan et al.

The Examiner respectfully traverses the Applicant's arguments. The Examiner notes that the stopper cells **245** as disclosed in *Gan et al.* are performing the functional equivalent of what a cover would do by preventing that area of an ASIC from being used for any other purpose. It is further noted that the *Gan et al.* reference discloses, ***(Col. 6 Lines 17-18,*** *They force a place-and-route tool to route a selected signal path through a particular physical location.)* In other words, the area denoted by the stopper cells cannot be used for any other purpose and the place-and-route tool must used that *"covered"* area for the purpose designated by the designer, *using the stopper cells*.

The Examiner has found Applicant's arguments to be unpersuasive and upholds the earlier rejections of claims 1-23.

## ***Claim Interpretations***

**3.** The broadest most reasonable interpretations, consistent with the specification, has been afforded the claim limitations. The following limitations have been interpreted as follows:

**Pre-cell**: The area in the core of the chip that is utilized when the area available on the perimeter of a chip is not sufficient to support the function of an I/O cell, know in the art per applicant's statements in the related prior art section, see page 4, lines 23-27, for example.

**Main-cell**: Located on the perimeter of the chip for I/O that is interconnected with the pre-cell located in the core of chip thereby providing I/O cells that are divided into perimeter areas and core areas. The I/O areas are divided into two or more cells interconnected between the main cell area and the pre-cell area, know in the art per applicant's statements in the related prior art section, see page 4, line 28-page 5, line 12, for example.

**Virtual cover or cover model:** Prevents the area of the core of the IC from being used for other purposes, covers each pre-cell, provides for adjusting the timing of the signals to compensate for the input/output cell being divided into two areas, see page 7 lines 12 et seq.

**Proprietary format:** Any manufacturer's proprietary format, for example NEC or Xilinx.

## *Claim Rejections - 35 U.S.C. § 102*

**4.** The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

**5.** Claims 1-23 are rejected under 35 U.S.C. §102(e) as being anticipated by Gan et al.

**6.** Taking claim 1, for example, teaches a computer program product, encoded in computer readable media, the computer program product for designing an integrated circuit chip, comprising: (abstract, Figures 2 and 3, col. 2, liens 25 et seq., col. 3, lines 55 et seq.)

a first set of instructions, executable on a computer system, the first set of

instructions configured to model an input/output cell located on the perimeter of an integrated circuit, the model of the input/output cell further comprising:

a model of a main cell; and (standard block 210)

a model of a pre-cell; and (phantom block 220, 230 )

a second set of instructions, executable on a computer system, the second set of instructions configured to model a cover wherein the cover (place-holding cell or "stopper cell", 245) prevents an area occupied by the pre-cell ("phantom blocks 220 and 230 are defined within respective bounding boxes 235 and 240, where "Bonding box" defines the area) from being used for any other purpose in the model, see col. 4, lines 6-45, for example.

As to claim 2, the computer program product as recited in claim 1, further comprising:

a third set of instructions, executable on a computer system, the third set of instructions configured to adjust the timing of the main-cell and pre-cell, wherein the timing adjustment to the main cell and pre-cell approximates the timing of a input/output cell is taught in Gan et al. at col. 4, lines 46 et seq., for example.

As to claim 3, the computer program product as recited in claim 1, wherein the first cover is used to cover a first pre-cell, further comprising:

a second pre-cell, wherein a single input/output cell is modeled with a main-cell, a first pre-cell and a second pre-cell, wherein the first cover prevents use of the area of the first pre-cell and the second cover prevents use of the area covered by the second pre-cell is taught in Gan et al. at col. 4, lines 29 et seq., for example.

As to claim 4, the computer program product as recited in claim 1, the computer program product further comprising: a database, wherein the database stores a netlist is taught in Gan et al. at col. 4, lines 61 et seq., for example.

As to claim 5, the computer program product as recited in claim 1, the computer program product further comprising:

a third set of instructions, the third set of instructions configured to convert a netlist to a proprietary format (Xilinx, for example) is taught in Gan et al. at col. 5, lines 1 et seq.

As to claim 6, the computer program product as recited in claim 1, further comprising:

a third set of instructions, the third set of instructions configured to flatten a netlist by reading a description of the function of a cell and listing each function of the cell individually, wherein reading a description of the function of a cell and listing each function of the cell individually is taught in Gan et al. at col. 5, lines 1 et seq., col. 5, lines 14 et seq., col. 6, lines 16 et seq., col. 6, lines 34 et seq., for example.

As to claim 7, the computer program product as recited in claim 1, further comprising:

a third set of instructions, the set of instructions configured to identify the location of each pin in an integrated circuit is taught in Gan et al. at col. 5, lines 1 et seq., LEF, for example.

As to claim 8, the computer program product as recited in claim 1, further comprising:

a third set of instructions, the third set of instructions configured to identify the location of each cell in an integrated circuit is taught in Gan et al. at col. 5, lines 1 et seq. , DEF, for example.

Claims 9-23 are rejected based upon the same reasoning as claims 1-8, *supra*. Claims 9-23 recite method and apparatus claims reciting the same limitations as claims 1-8 and taught in

Gan et al., see abstract, Figures 2 and 3, col. 2, lines 25 et seq., col. 3, lines 55 et seq., col. 5, lines 1 et seq., for exemplary teachings to be inclusive of citations referencing specific limitations as provided in the analysis of claims 1-8.

## ***Conclusion***

**8.** Claims 1-23 are rejected.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

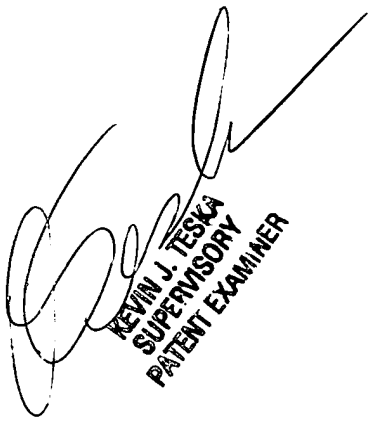
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

## CONTACT INFORMATION

**9.** Any inquiry concerning this communication or earlier communications from the examiner should be directed to William D. Thomson whose telephone number is 703-305-0022. The examiner can normally be reached on 8:30-3:30 Tuesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).




William Thomson
Primary Examiner
A.U. 2123
Technology Center 2100
August 11, 2004